CLAIMS

1. (Currently amended) A system for processing a set of data bits ~~using a subset of a recurring sequence of scrambler bits~~, ~~the system~~ comprising:

~~receiving means for receiving said set of data bits;~~

storage means for storing ~~said~~ the set of data bits;

digital logic means for determining ~~an appropriate~~ a subset of ~~said~~ a serial sequence of scramble bits ~~based, at least in part, on a generator polynomial and one or more bits from a prior appropriate subset~~ by applying a generating polynomial to the serial sequence of scramble bits;

generating means for generating ~~said appropriate subset based, at least in part, on said generator polynomial and said prior appropriate subset wherein, for each bit of said set of data bits, at least one bit of said appropriate subset is associated therewith~~ the subset responsive to an immediately preceding state of the subset; and

digital operation means for performing a bitwise parallel digital operation between ~~said appropriate subset and each bit of said set of data bits and said at least one bit of said appropriate subset associated therewith~~ each bit of the set of data bits with at least one corresponding bit of the subset to produce an output set of data bits;

where a number of bits in the subset corresponds to a periodicity of the serial sequence of scramble bits.

2. (Currently amended) A system according to claim 1 where~~in said~~ the system ~~scrambles~~ is adapted to scramble ~~said~~ the set of data bits using ~~said appropriate subset of scramble bits~~ the subset.

3. (Currently amended) A system according to claim 1 where~~in said~~ the system ~~descrambles~~ is adapted to scramble ~~said~~ the set of data bits using ~~said appropriate subset of scramble bits~~ the subset.

4. (Currently amended) A system according to claim 1 ~~wherein said~~ comprising receiving means ~~comprises a multiplexer~~ including multiplexing means for receiving the serial sequence of scramble bits.

5. (Canceled)

6. (Currently amended) A system according to claim ~~5~~ 1 where~~in said~~ the digital logic means ~~is a~~ includes combinational logic ~~circuit~~ means for logically manipulating the serial sequence of scramble bits.

7. (Currently amended) A system according to claim 1 where~~in said~~ the bitwise parallel operation ~~is~~ includes a bitwise parallel XOR operation.

8. (Currently amended) A digital scrambler/descrambler using a subset of a ~~securing~~ serial sequence of scrambler bits, the scrambler/descrambler comprising:

selection means for selecting between a first set of data bits to be scrambled and a second set of data bits to be descrambled;

digital logic means for determining ~~an appropriate~~ a subset of ~~said~~ the serial sequence of scrambler bits, ~~said appropriate~~ the subset being determined based on an immediately preceding subset of ~~said~~ the serial sequence of scrambler bits;

digital operation means for executing a bitwise parallel digital operation between ~~said appropriate~~ the subset and either ~~said~~ the first or ~~said~~ the second set of data bits;

where a number of bits in the subset corresponds to a periodicity of the serial sequence of scramble bits.

9. (Currently amended) A digital scrambler/descrambler according to claim 8 where~~in said~~ the bitwise parallel digital operation ~~is~~ includes a bitwise parallel XOR operation.

10. (Currently amended) A digital scrambler/descrambler according to claim 8 where~~in said~~ the selection means ~~is~~ includes a multiplexer.

11. (Currently amended) A digital scrambler/descrambler according to claim 8 where~~in said~~ the digital logic means ~~is~~ includes a combinational logic circuit.

12. (Currently amended) A digital scrambler/descrambler according to claim 11 where~~in said~~ the digital logic means includes a digital storage means for storing ~~said~~ the immediately preceding subset.

13. (Currently amended) A method of processing a plurality of data bits using a subset of a recurring serial sequence of scrambler bits, the method comprising:

a) ~~receiving and~~ storing in parallel ~~said~~ the plurality of data bits;

b) determining a ~~an appropriate~~ subset of ~~said~~ the recurring serial sequence of scrambler bits based on an immediately preceding subset of ~~said~~ the recurring serial sequence of scrambler bits;

c) generating ~~said appropriate~~ the subset where~~in~~, for each bit of ~~said~~ the plurality of data bits, at least one bit of ~~said~~ the appropriate subset is associated therewith;

~~d) loading said appropriate subset in a storage means;~~ and

~~e)~~ d) performing a bitwise parallel XOR operation between ~~said appropriate subset and~~ each bit of ~~said~~ the plurality of data bits and ~~said~~ the at least one bit of ~~said appropriate~~ the subset associated therewith to produce an output set of data bits;

where a number of bits in the subset corresponds to a periodicity of the recurring serial sequence of scramble bits.

14. (Currently amended) A method according to claim 13 ~~wherein step b) is accomplished by~~ comprising performing logical operations between specific scrambler bits of ~~said~~ the immediately preceding subset.

15. (Currently amended) A method according to claim 13 ~~wherein step c) is accomplished by~~ comprising performing logical operations between specific scrambler bits of ~~said~~ the immediately preceding subset.

16. (Currently amended) A method according to claim 13 ~~wherein said storage means is~~ comprising loading the subset in a register.

17. (New) A scrambler comprising:

a register block to store a current state of a subset of a recurring serial sequence of scramble bits;

a predict logic block to generate the current state of the subset responsive an immediately preceding state of the subset; and

a scramble logic block to scramble a data set in parallel with the current state of the subset;

where the number of bits in the current state of the subset corresponds to a periodicity of the recurring serial sequence of scramble bits.

18. (New) The scrambler of claim 17 comprising a multiplexer block to multiplex a serial version of the data set to create a parallel version of the data set.

19. (New) The scrambler of claim 17 where the predict logic block or the scramble logic block includes a corresponding plurality of parallel combinational sub blocks.

20. (New) The scrambler of claim 17 where the predict logic block is configured to determine the current state of the subset by applying a generator polynomial defined in the IEEE 802.11a.